What we claim is:

1. A process for forming at least one transistor on a substrate, which process comprises depositing on the substrate at least one layer of semiconductor material, wherein the substrate comprises a polyphenylene polyimide.

2. A process according to claim 1 wherein the polyphenylene polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid.

3. A process according to claim 2 wherein the polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid and an α,ω-alkanediamine.

4. A process according to claim 1 wherein a passivating layer is deposited on the substrate before the semiconductor material is deposited thereon.

5. A process according to claim 4 wherein the passivating layer comprises silicon dioxide or aluminum nitride.

6. A process according to claim 4 wherein the passivating layer has a thickness in the range of about 20 to about 100 nm.

7. A process according to claim 4 wherein the passivating layer is deposited on both surfaces of the substrate.

8. A process according to claim 4 wherein the substrate is heated to a temperature greater than about 150°C for a period of at least about 1 minute before deposition of the passivating layer.

9. A process according to claim 4 wherein the substrate is heated to a temperature greater than about 250°C for a period of at least about 5 hours after deposition of the passivating layer.

10. A process according to claim 1 wherein the substrate is heated to a temperature greater than about 250°C for a period of at least about 1 hour before deposition of the semiconductor material.

11. A process according to claim 1 wherein the substrate comprises a metal layer on the side thereof remote from the semiconductor material.

12. A process according to claim 11 wherein the metal layer has walls defining apertures extending through the metal layer.

13. A process according to claim 1 wherein the deposition of the semiconductor material is effected at a temperature in excess of about 300°C.

14. A process according to claim 1 wherein a metal layer is deposited upon the substrate on the same side thereof as the semiconductor material but prior to the deposition of the semiconductor material.

15. A process according to claim 14 wherein the metal layer comprises chromium.

16. A process according to claim 14 wherein the metal layer is deposited as a continuous film and is thereafter patterned prior to deposition of the semiconductor material thereon.

17. A process according to claim 14 wherein a layer of dielectric material is deposited over the metal layer prior to the deposition of the semiconductor material.

18. A process according to claim 17 wherein the dielectric layer comprises silicon nitride.

19. A process according to claim 1 wherein the dielectric layer is deposited by plasma enhanced chemical vapor deposition.

20. A process according to claim 1 wherein the semiconductor material comprises amorphous silicon.

21. A process according to claim 20 wherein the semiconductor material is deposited by plasma enhanced chemical vapor deposition.

22. A process according to claim 20 wherein the amorphous silicon is not patterned so that it extends continuously between at least some pairs of adjacent transistors

23. A process according to claim 20 wherein the semiconductor material further comprises a layer of n-type silicon deposited over the amorphous silicon.

24. A process according to claim 23 wherein a continuous layer of the n-type silicon is deposited over the amorphous silicon, a patterned layer of metal is thereafter formed over the n-type silicon, and the resultant structure is thereafter etched to remove portions of the n-type silicon not covered by the patterned layer of metal.

25. A process according to claim 1 wherein deposition of the semiconductor material is effected on a continuous web of substrate.

26. A substrate comprising a polyphenylene polyimide, the substrate bearing at least one transistor

27. A substrate according to claim 26 wherein the polyphenylene polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid.

28. A substrate according to claim 27 wherein the polyimide is a derivative of biphenyl-3,3',4,4'-tetracarboxylic acid and an α,ω-alkanediamine.

29. A substrate according to claim 26 having a passivating layer between the substrate and the transistor.

30. A substrate according to claim 27 having a metal layer on the side thereof remote from the transistor.

31. A substrate according to claim 27 wherein the transistor comprises at least one amorphous silicon layer.

32. A substrate according to claim 31 bearing at least at least two transistors, each of the transistors comprising at least one amorphous silicon layer and the silicon layer extending continuously between the two transistors.

33. A substrate according to claim 27 wherein the transistor further comprises at least one n-type silicon layer in contact with the amorphous silicon layer.